WHAT IS CLAIMED IS:

1. A semiconductor multi-chip package comprising:

a package substrate including a surface having a plurality of bonding tips formed thereon; and

two or more semiconductor chips mounted on the substrate surface, the two or more semiconductor chips each including:

a semiconductor substrate having integrated circuits formed on a cell region and a peripheral circuit region adjacent to each other;

a bond pad-wiring pattern formed on the semiconductor substrate; and

a pad-rearrangement pattern electrically connected to the bond pad-wiring pattern, the pad-rearrangement pattern including bond pads disposed over at least a part of the cell region,

wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate,

wherein each bonding tip is electrically connected to a corresponding one of the bond pads.

2. The multi-chip package of claim 1, wherein the two or more chips are disposed next to each other.

3. The multi-chip package of claim 1, wherein the two or more chips are vertically stacked.

4. The multi-chip package of claim 1, wherein the two or more chips comprise the same type of chips.

5. The multi-chip package of claim 1, wherein the two or more chips comprise at least a lower chip and an upper chip, the upper chip disposed over the lower chip, and wherein the width of the upper chip is smaller than the width of the lower chip.

6. The multi-chip package of claim 1, wherein one of the two or more chips is a memory chip and the other chip is a non-memory chip.

7. The multi-chip package of claim 1, wherein one of the two or more chips is a DRAM and the other chip is a flash memory.

8. The multi-chip package of claim 1, wherein the bond pads are formed along sides of the semiconductor substrate.

9. The multi-chip package of claim 1, wherein a portion of the pad-rearrangement pattern extends substantially from the center region of the semiconductor substrate toward an edge of the semiconductor substrate.

10. The multi-chip package of claim 1, wherein the bond pad-wiring pattern is form on a portion of the peripheral circuit region and extends across a portion of the cell region.

11. The multi-chip package of claim 1, wherein the bond pad-wiring pattern is formed entirely within the peripheral circuit region.

12. A semiconductor multi-chip package, comprising:

a lead frame having a front surface and a back surface;

a first chip having an upper surface and a lower surface, the upper surface of the first chip disposed under the back surface of the lead frame, the first chip having bond pads formed substantially along a center region of the upper surface; and

a second chip having an upper surface and a lower surface, the upper surface of the second chip disposed under the lower surface of the first chip, the second chip including:

a semiconductor substrate having integrated circuits formed on a cell region and a peripheral circuit region adjacent to each other;

a bond pad-wiring pattern formed on the semiconductor substrate; and

a pad-rearrangement pattern electrically connected to the bond pad-wiring pattern, the pad-rearrangement pattern including bond pads disposed over at least a part of the cell region, wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate,

wherein the bond pads of the first chip are electrically connected to the lead frame, and wherein the bond pads of the second chip are electrically connected to the lead frame.

13. The multi-chip package of claim 12, wherein the bond pads are formed along sides of the semiconductor substrate.

14. The multi-chip package of claim 12, wherein a portion of the pad-rearrangement pattern extends substantially from the center region of the semiconductor substrate toward an edge of the semiconductor substrate.

15. The multi-chip package of claim 12, wherein the bond pad-wiring pattern is form on a portion of the peripheral circuit region and extends across a portion of the cell region.

16. The multi-chip package of claim 12, wherein the bond pad-wiring pattern is formed entirely within the peripheral circuit region.

17. A semiconductor multi-chip package comprising:

a lead frame including a die pad and a lead, the die pad having a front surface and a back surface; and

a first chip disposed over the front surface of the die pad and a second chip disposed over the back surface of the die pad, the first and the second chip each including:

a semiconductor substrate having integrated circuits formed on a cell region and a peripheral circuit region adjacent to each other;

a bond pad-wiring pattern formed on the semiconductor substrate; and

a pad-rearrangement pattern electrically connected to the bond pad-wiring pattern, the pad-rearrangement pattern including bond pads disposed over at least a part of the cell region,

wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate,

wherein the bond pads of the first and second chips are each electrically connected to the lead.

18. The multi-chip package of claim 17, further comprising an additional chip disposed over at least one of the first and second chips, the additional chip having peripheral pads, the peripheral pads are electrically connected to the lead.

19. The multi-chip package of claim 17, wherein the width of the additional chip is smaller than the width of the first or second chip.

20. The multi-chip package of claim 17, wherein the bond pads are formed along sides of the semiconductor substrate.

21. The multi-chip package of claim 17, wherein a portion of the pad-rearrangement pattern extends substantially from the center region of the semiconductor substrate toward an edge of the semiconductor substrate.

22. The multi-chip package of claim 17, wherein the bond pad-wiring pattern is form on a portion of the peripheral circuit region and extends across a portion of the cell region.

23. The multi-chip package of claim 17, wherein the bond pad-wiring pattern is formed entirely within the peripheral circuit region.